Investigation of Millisecond-long ASETs in Linear ICs: Case Study of the LM6144 Op Amp

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Motivation

- **We have encountered a class of Analog Single-Event Transients with an unprecedented characteristic:**

  - pulse durations up to 3 orders of magnitude longer than anything previously reported in the literature

- **Until now, the most severe pulse durations recorded:**
  - few tens of μs maximum

- **Surprising recent ion-beam data on the LM6144 op amp:**

  - ASETS with pulse durations from hundreds of μs to several ms (LDPs)

- **Chronology of the investigation:**

  - first observations by M. Savage at Texas A&M cyclotron
  - corroborated by Alcatel Aerospace at RADECS 2003
  - identified by S. Buchner and D. McMorrow with NRL laser
  - additional experiments by D. McMorrow and V. Pouget at IXL labs
  - ASET simulation and LDP modeling by Vanderbilt

- **We are presenting our understanding of the LDP phenomenon and its mechanisms using the experimental observations**

Outline

- **Presentation of the LDPs experimental data:**
  - Heavy-ion tests
  - IXL laser data
  - NRL investigations on LDP triggering conditions
- **Circuit theory on the sensitive part of the circuit:**
  - to understand the interaction between SETs and possible loss of functionality observed in the LM6144
- **Circuit simulation results explaining the LDP triggering conditions and variation in their severity**

Heavy-Ion Tests

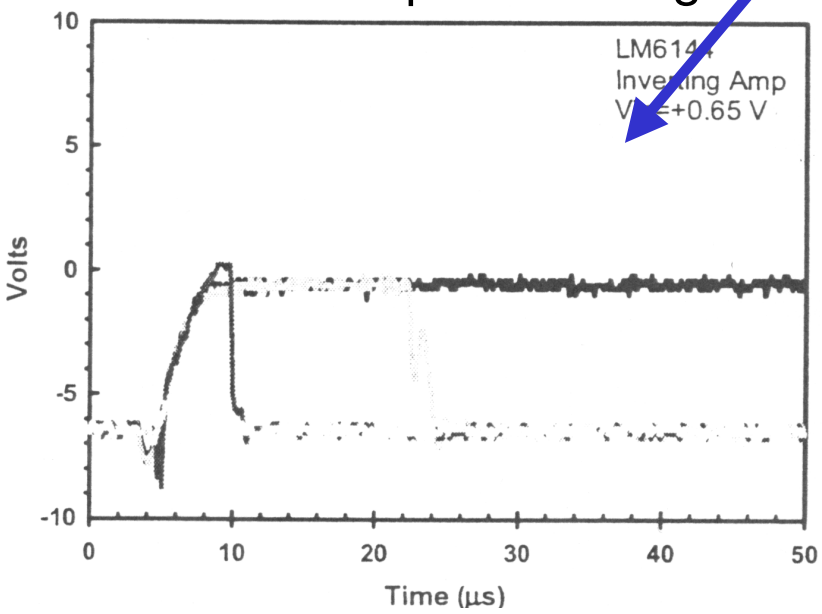
Texas A&M Cyclotron facility - Broadbeam results

Vanderbilt Engineering

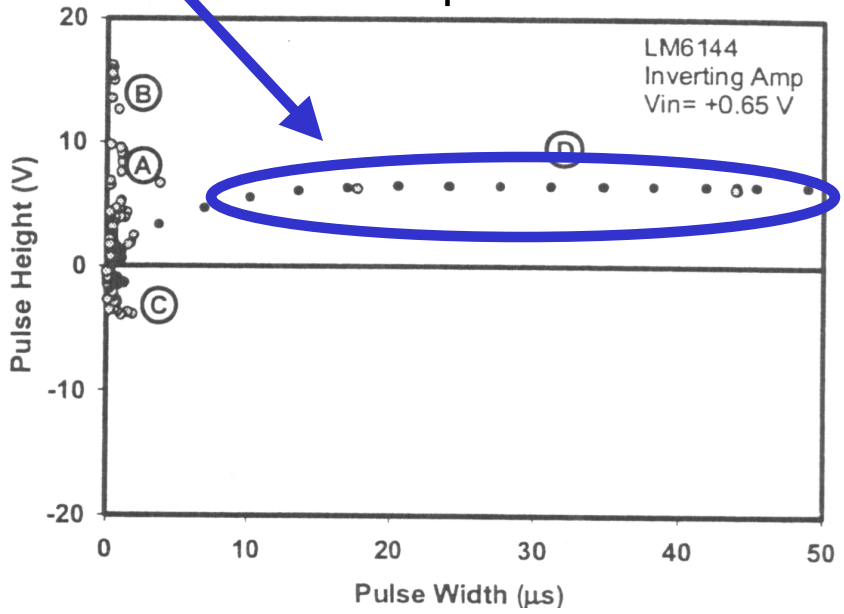
- **Heavy-Ion test on the LM6144 revealed the possible occurrence of ASETs with pulse widths in the millisecond range (Subset D):**
  - previously unseen
  - serious implications in space systems, since they are more likely to propagate and much harder to filter out

Subset D

Oscilloscope recordings



FWHM representation



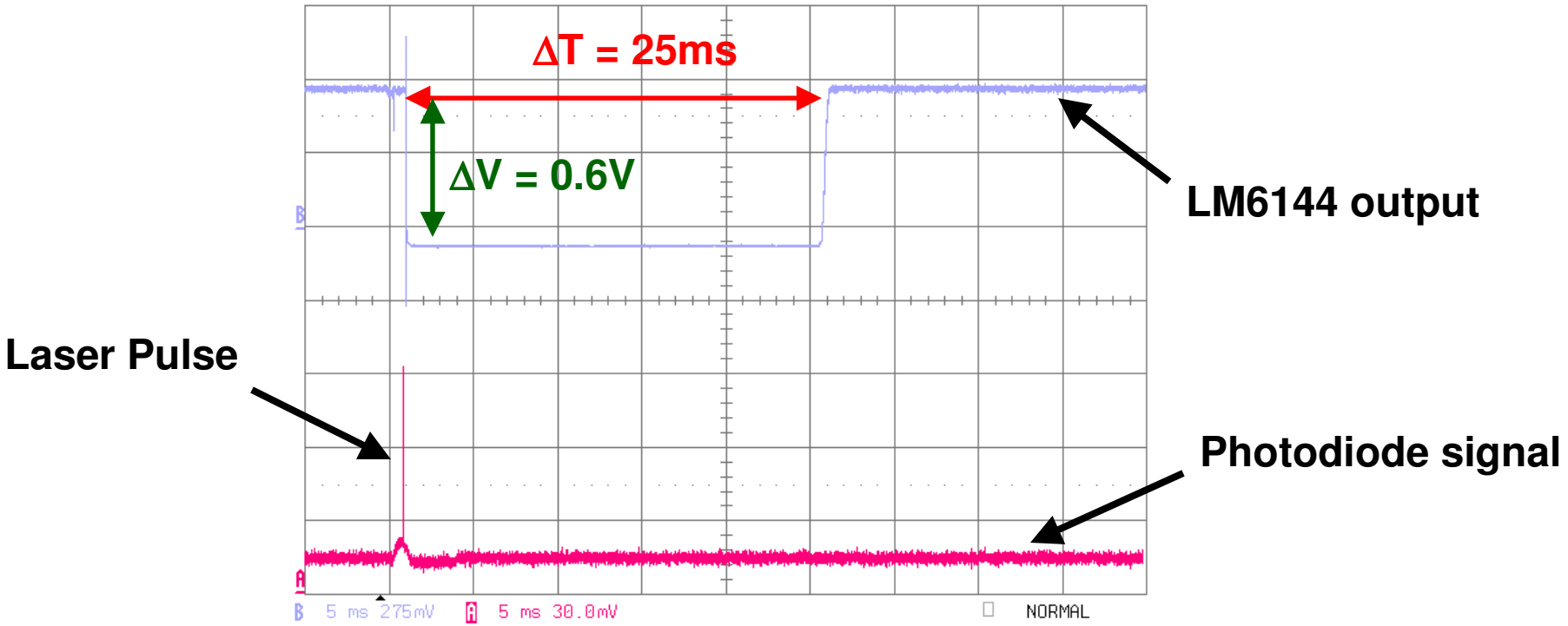
M. W. Savage et al., "Characterization of SET Response of the LM124A, the LM111, and the LM6144," 2003 IEEE Radiation Effects Data Workshop, pp. 121-126

Laser Tests

IXL Labs - Pulsed laser results

- **Long Duration Pulses (LDPs) observation:**
  - Test condition: Inverter, Vin=60mV, Av=10, Vcc= 10V, Vss=-10V

- **Strong dependence of recovery time on power supply voltages:**
  - ± 10V ⇒ 25ms pulse
  - ± 7.5V ⇒ 45ms pulse
  - ± 5V ⇒ 100ms pulse



Exp. D. McMorrow and V. Pouget

Laser Tests

Naval Research Laboratories - Details of triggering conditions

- **To trigger an LDP, a relatively high laser intensity is needed:**
  - agrees with the heavy-ion data in which LDPs where observed only for the high-LET ions of Au and Xe

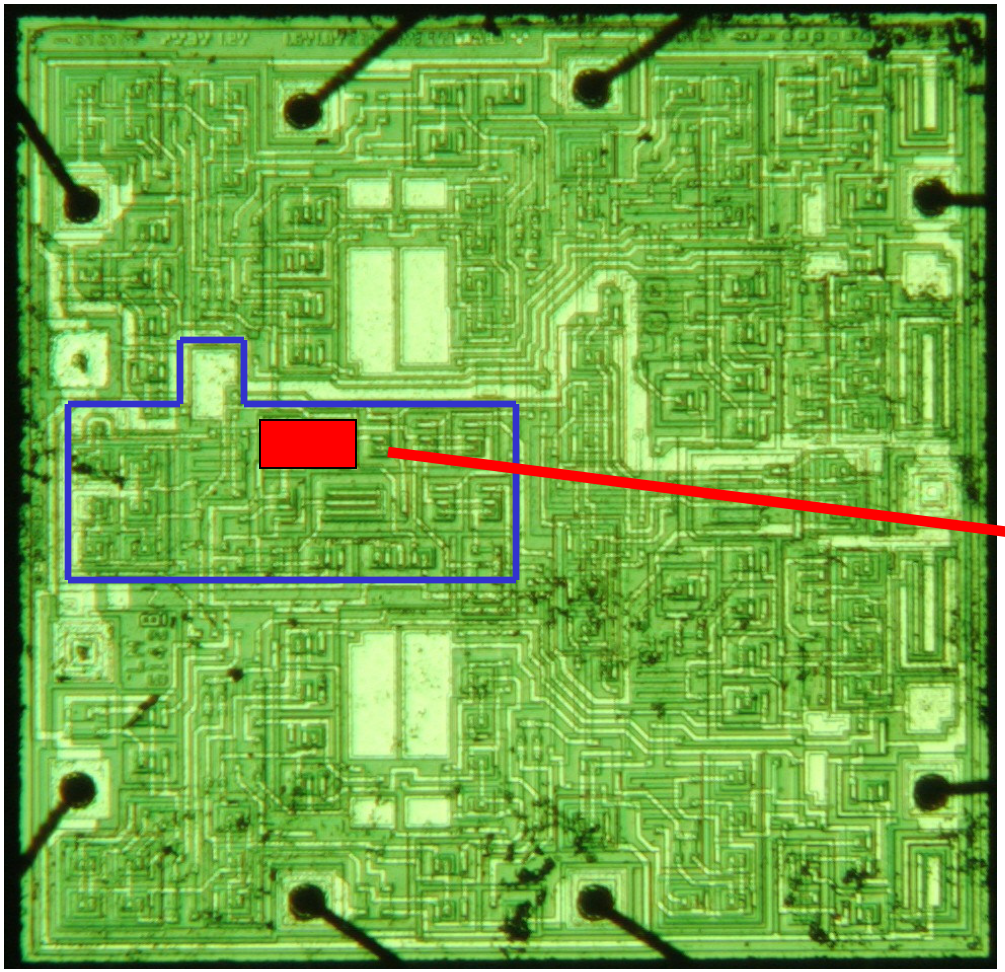
- **Once the LDP has been generated, a small amount of light can significantly delay the circuit recovery:**
  - illuminator
  - scattered light in the laser beam
  - room lights

- **If the circuit is experiencing an LDP, a laser strike adjacent to the sensitive region will remove it**

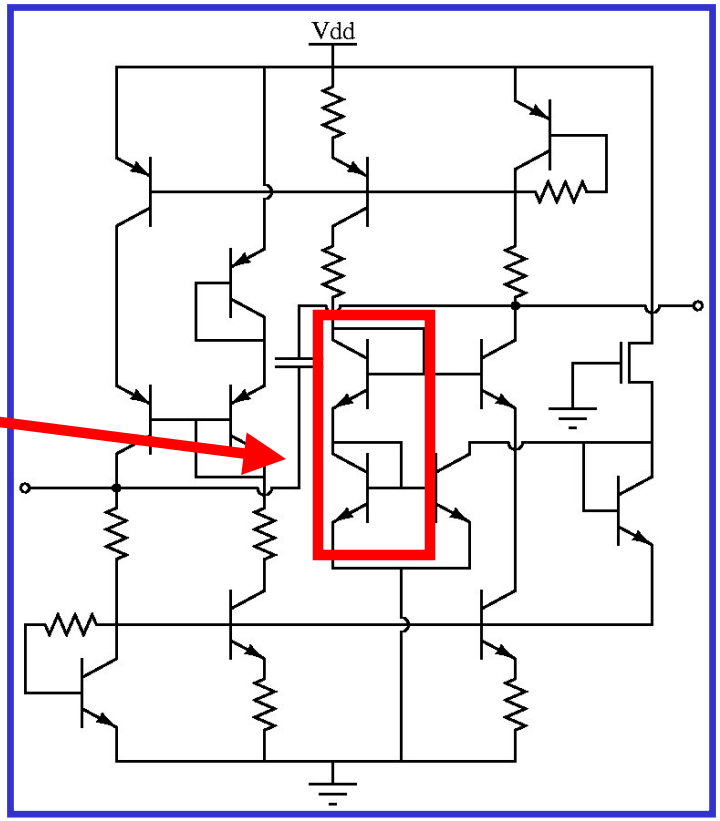
Exp. S. Buchner and D. McMorrow

Circuit Modeling of the Sensitive Area

- **The laser scan of the LM6144 IC revealed a localized sensitive area:**
  - 2 NPN transistors of the Bias/Startup circuitry



Bias/Startup schematic



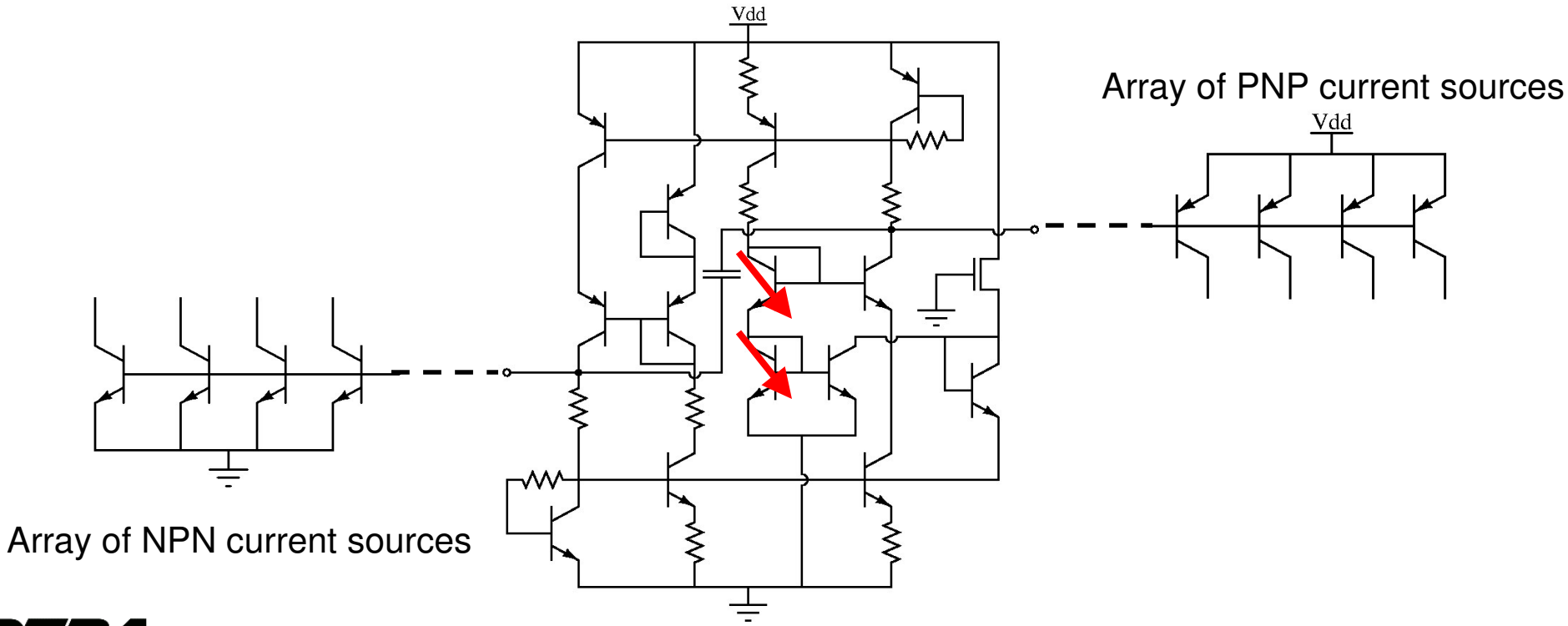
Exp. S. Buchner and D. McMorrow

Failure Mechanism Origin

Destabilization of the bias/startup circuitry

- **<u>Startup circuitry</u>: used for circuits that may present two or more stable operating states:**
  - power can be turned ON but transistors can set themselves in an operating mode different (but stable) from the one required by the designer

- **The injection of current pulses at the location identified by the laser acts as a second startup current:**
  - forces the biasing circuitry into an undesirable operating state



Consequence of Control-Bias Perturbation

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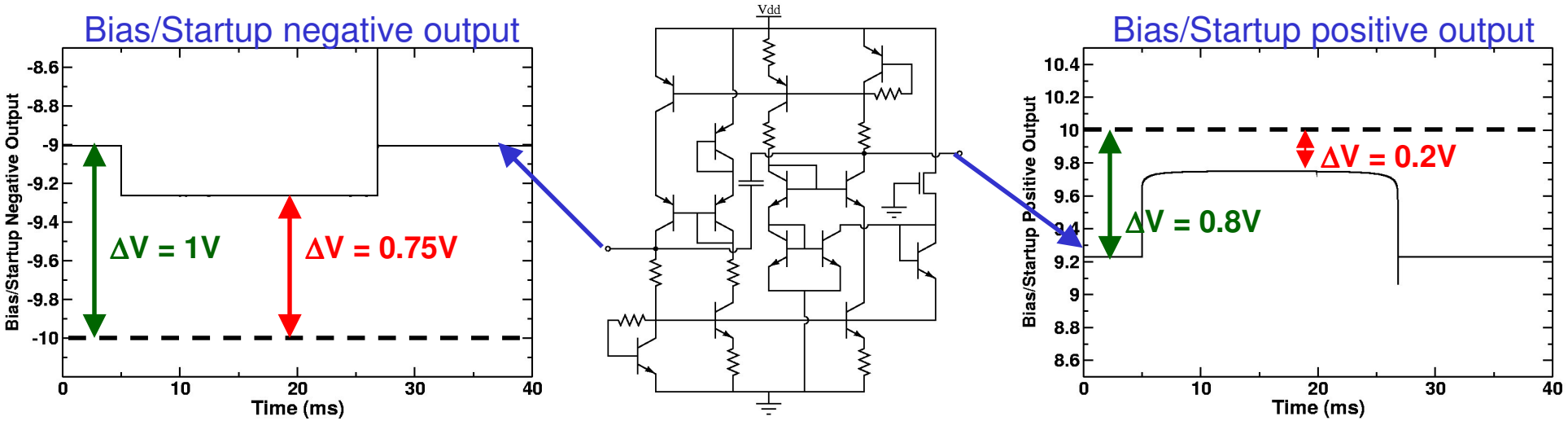
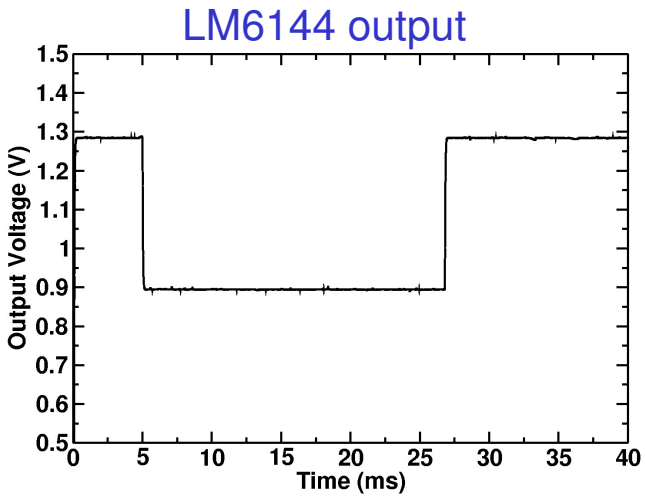
- **The voltages controlling the NPN and PNP biasing current sources are severely altered:**
  - new SET-induced voltages are insufficient to maintain the base-emitter junction forward-biased, resulting in turning some of them OFF



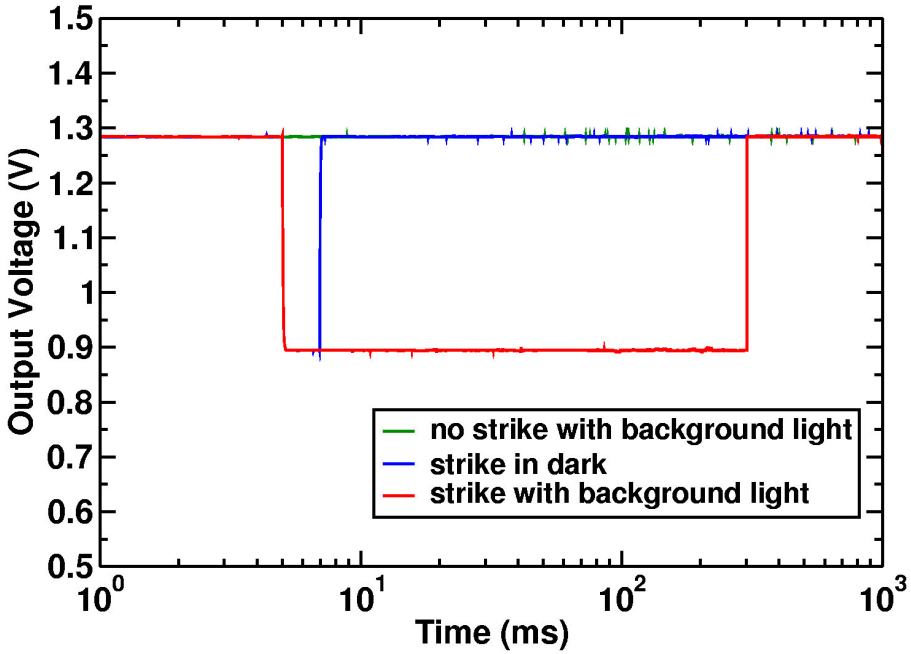


Laser pulse characteristics:
CE: 7mA x 4.3ns= 30pC

Failure Mechanism Analysis 1

Interference of parasitic light in IC recovery

- **In addition to the laser current pulse, the exposure to background light was simulated as a very low photocurrent collected across the CB junction of the sensitive transistors**



Laser pulse characteristics:
CE: 7mA x 4ns= 28pC

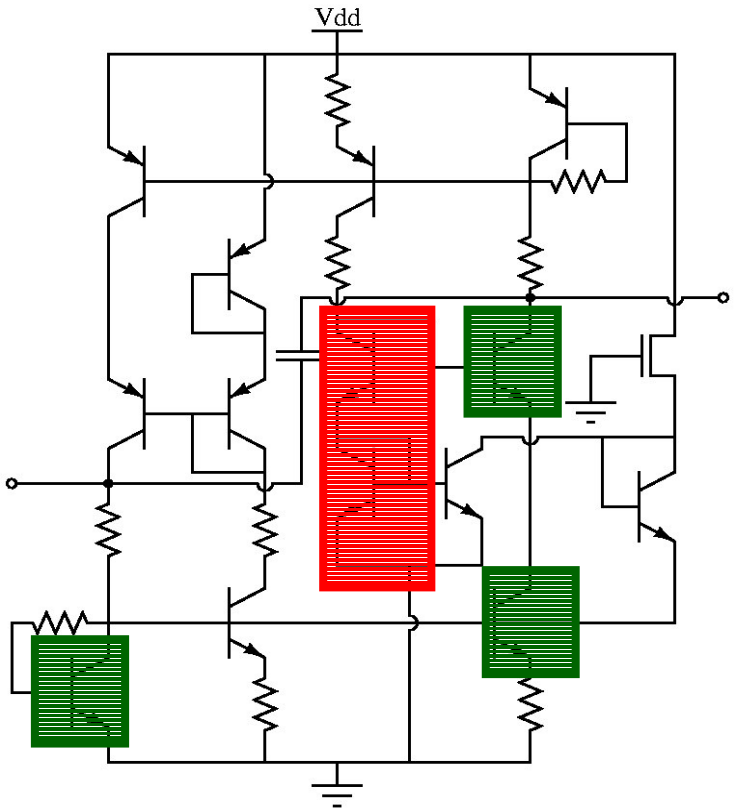
Background photocurrent characteristics:
CB: 1nA x 50ms

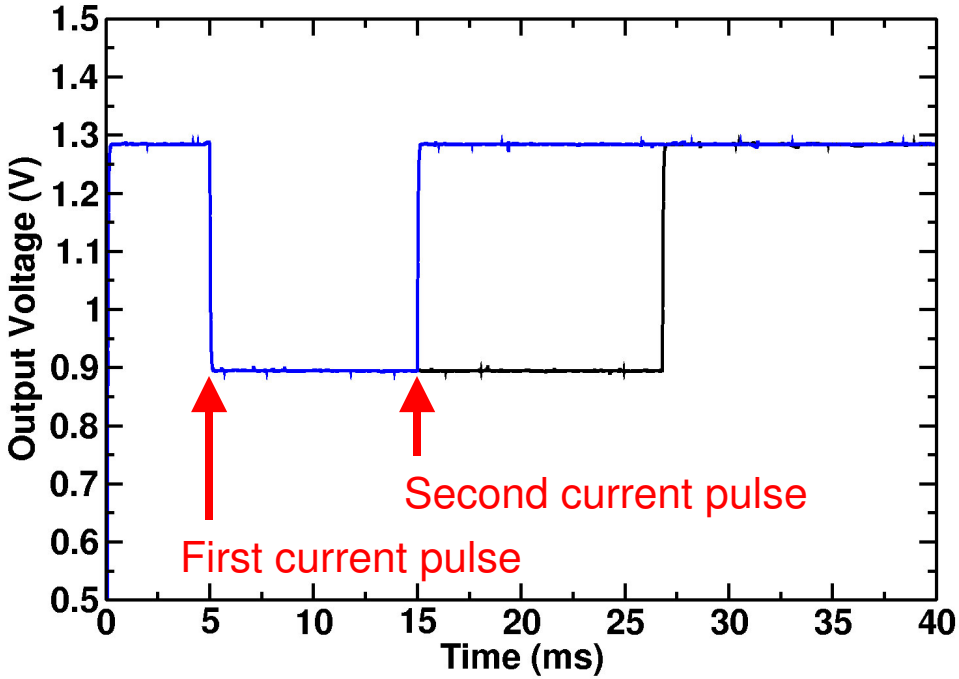
- **The photocurrent due to background illumination adds to the photocurrent from laser strike:**
  - delays the charge leakage
  - longer time for recovery

- **May corrupt experimental tests on delidded parts**

Failure Mechanism Analysis 2
Laser–induced LDP recovery

- **Hits on the immediate neighbors of the sensitive transistors improve the current leakage paths:**
  - induce a quasi-immediate recovery of the circuit output





Failure Mechanism Analysis 3

LDP width dependence on power supplies

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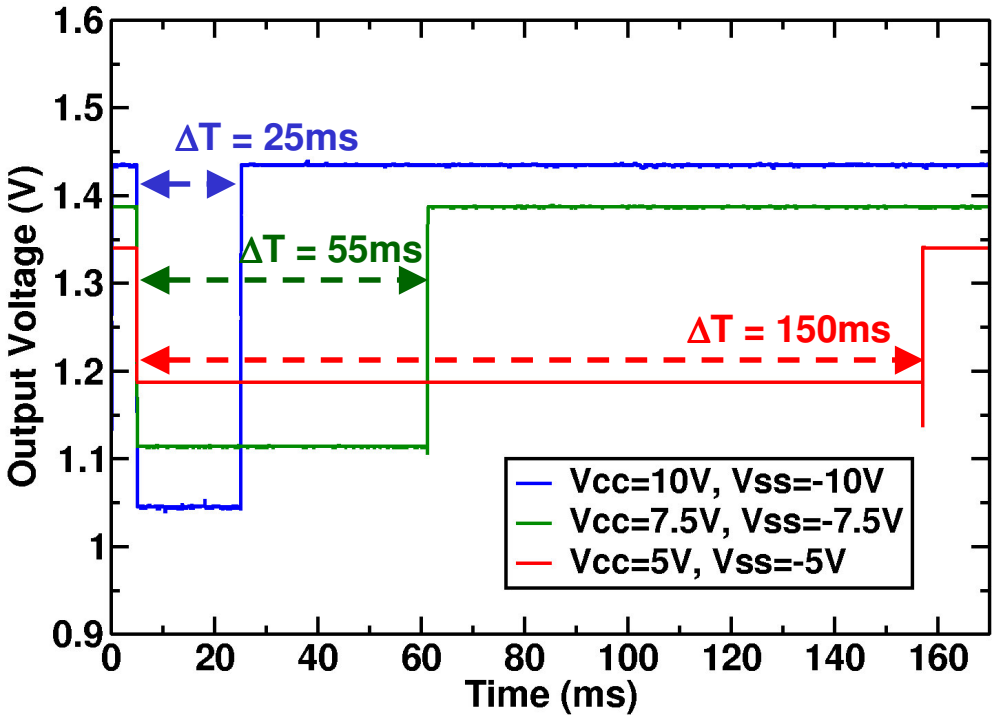
- **The transistors operate at higher currents when the power supply voltages are increased:**

  - photocurrents generated by laser strikes induce a relatively smaller perturbation
  - the bias/startup circuitry recovers faster: shorter LDPs



Conclusions

- A new category of ASETs has been investigated by the DTRA team:
  - observed during heavy-ion beam experiments
  - localized by laser tests
- Used circuit simulation to model the phenomenon and uncover its causes
- The hardness assurance methodology for analog ICs proposed by Marec et al. (RADECS conference 2001) and based on former worst-case ASET characteristics may need to be updated (cf. R. Pease HEART 2004)
- This work will be presented in more details (specifically the experimental part) in the NSREC 2004 abstract